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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/653,583	08/31/2000	Yoshiro Mikami	503.35282CX2	6649	
20457 ANTONELLI	7590 12/28/2007 TERRY STOUT & KRA	EXAMINER			
1300 NORTH	ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-3873			PIZIALI, JEFFREY J	
				PAPER NUMBER	
			2629		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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		Application No.	Applicant(s)	
		09/653,583	MIKAMI ET AL.	
Office Action Summary		Examiner	Art Unit	
	•	Jeff Piziali	2629	
	The MAILING DATE of this communication a or Reply	ppears on the cover sheet w	ith the correspondence address	
WHIC - Exter after - If NO - Failur Any r	ORTENED STATUTORY PERIOD FOR REF CHEVER IS LONGER, FROM THE MAILING asions of time may be available under the provisions of 37 CFR SIX (6) MONTHS from the mailing date of this communication. In period for reply is specified above, the maximum statutory perion are to reply within the set or extended period for reply will, by state tell received by the Office later than three months after the mailed patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNI 1.136(a). In no event, however, may a od will apply and will expire SIX (6) MOR tute, cause the application to become Al	CATION. reply be timely filed NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).	
tatus				
1)🖂	Responsive to communication(s) filed on <u>15</u>	October 2007.		
2a)□				
3)	Since this application is in condition for allow	vance except for formal mat	ters, prosecution as to the merits is	
	closed in accordance with the practice unde	r <i>Ex parte Quayle</i> , 1935 C.D). 11, 453 O.G. 213.	
ispositi	on of Claims	•		
4) 🛛	Claim(s) <u>9,23,24,30-37 and 40-45</u> is/are per	nding in the application.		
	4a) Of the above claim(s) <u>9,23,24,32-35 and</u>	· -	onsideration.	
	Claim(s) is/are allowed.			
6)🛛	Claim(s) 30,31,36 and 40-45 is/are rejected.			
7)	Claim(s) is/are objected to.			
8)	Claim(s) are subject to restriction and	d/or election requirement.		
pplicati	on Papers			
	The specification is objected to by the Exami	iner.		
	The drawing(s) filed on <u>31 August 2000</u> is/ar		bjected to by the Examiner.	
,—	Applicant may not request that any objection to the			
	Replacement drawing sheet(s) including the corr	ection is required if the drawing	g(s) is objected to. See 37 CFR 1.121(d).	
11)	The oath or declaration is objected to by the	Examiner. Note the attache	d Office Action or form PTO-152.	
riority u	ınder 35 U.S.C. § 119			
	Acknowledgment is made of a claim for forei All b) Some * c) None of:		§ 119(a)-(d) or (f).	
	 Certified copies of the priority docume Certified copies of the priority docume 		Application No. 08/820 835	
	3. ☐ Copies of the certified copies of the pi		• •	
	application from the International Bure	•		
* S	See the attached detailed Office action for a li		received.	
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	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)		Summary (PTO-413) (s)/Mail Date	
) 🔲 Inform	mation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date		Informal Patent Application	

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 October 2007 has been entered.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 08/820,835, filed on 19 March 1997.

Terminal Disclaimer

3. The terminal disclaimer filed on 29 January 2003 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,115,017 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Election/Restrictions

4. Applicants' election with traverse of Species I, Sub-Species A, Sub-Sub-Species 1 (i.e., claims 6, 27-31, 36, and 38-45) in the reply filed on 23 March 2007 is acknowledged. The

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traversal is on the ground(s) that, "the requirement does not relate to the claimed invention or illustrated species. For example, independent claim 6 and dependent claim 27, the only claims, which the Examiner considers to be properly under consideration, are written in an alternative format that either the drain or the source is connected to the corresponding signal electrode, a capacitor is at least partially formed by a portion of either the drain or the source of the thin film transistor, and that one electrode of the capacitor is formed of a same material as a material of either the drain or the source of the thin film transistor. The claims do not specify the drain or the source, as required by the Examiner in terms of the Species, Sub-Species and Sub-Sub-Species. Thus, claims 6 and 27 are generic claims" (see Page 10 of the 'Amendment' filed 23 March 2007).

This is not found persuasive, because the species are independent or distinct because claims to the different species recite the mutually exclusive characteristics (e.g., transistor drain or alternately source connections and material compositions) of such species. In addition, these species are not obvious variants of each other based on the current record.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

The requirement is still deemed proper and is therefore made FINAL.

5. Claims 9, 23, 24, 32-35, and 37 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, sub-species, and/or sub-sub-species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 23 March 2007.

6. Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claims 30, 31, 36, and 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Hamada et al (US 5,194,974)* in view of *Matsuda et al (US 5,352,907)*.

Regarding claim 30, Hamada discloses a liquid crystal display apparatus (see the abstract), having a pair of substrates of which at least one substrate is transparent (see Column 6, Line 15) and a liquid crystal layer sandwiched between the substrates (see Column 1, Lines 20-21), comprising: a plurality of scanning electrodes [Fig. 4; Y] formed on one of the substrates

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(see Column 5, Line 55); and a plurality of signal electrodes [Fig. 4; X] intersecting in a matrix form with said plurality of scanning electrodes (see Figure 2 and Column 5, Line 54); wherein the display apparatus further comprises, within each of the regions surrounded by said plurality of scanning electrodes and said plurality of signal electrodes: (a) a display data holding circuit [Fig. 4; TFT1 and C1] connected to a corresponding scanning electrode [Fig. 4; Y₁] and signal electrode [Fig. 4; X₁], for fetching and storing display data from a signal electrode in response to a scanning signal (see Column 6, Lines 54-55) for holding a display image [in C1] without updating the display data [in C2] while a power supply [Fig. 4; Vc] to the display apparatus is maintained (see Column 6, Lines 59-65); (b) a switching device [Fig. 4; TFT2] connected to said display data holding circuit and having a switching operation thereof controlled by the display data holding circuit (see Column 6, Lines 59-65); and (c) a display electrode [Fig. 4; C2] connected to said switching device (see Column 5, Lines 66-68); wherein said display data holding circuit includes a thin film transistor [Fig. 4; TFT1] having a gate connected to the corresponding scanning electrode and one of a drain and a source connected to the corresponding signal electrode, and a capacitor [Fig. 4; C1] at least partially formed by a portion of one of the drain and the source of said thin film transistor (see Column 5, Lines 53-65 and Column 7, Line 38 - Column 8, Line 45), wherein the drain of the thin film transistor of the display data holding circuit is connected to the corresponding signal electrode (see Fig. 4; Column 7, Line 38 -Column 8, Line 45), and the capacitor is at least partially formed by a portion of the drain of said thin film transistor (see Fig. 4; Column 7, Line 38 - Column 8, Line 45).

Hamada does not expressly disclose the display data holding circuit having one of a coplanar and an inverse stagger structure.

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However, Matsuda et al. discloses thin film transistor circuits of a coplanar as well as an inverse stagger structure (see Column 1, Lines 49-54).

Hamada and Matsuda are analogous art because they are from the shared inventive field of using thin film transistor circuits for controlling liquid crystal elements.

Therefore, it would have been obvious to one skilled in the art at the time of invention to use Matsuda's coplanar or inverse stagger structure with Hamada's display data holding circuit, so as to manufacture the liquid crystal display apparatus with conventional, well known TFT design techniques (see Matsuda: Column 1, Lines 49-54).

Regarding claim 31, Hamada discloses one electrode of the capacitor is formed of a same material as a material of the drain of said thin film transistor (see Fig. 4; Column 7, Line 38 - Column 8, Line 45).

Regarding claim 36, this claim is rejected by the reasoning applied in rejecting claims 30 and 31.

Regarding claim 40, this claim is rejected by the reasoning applied in rejecting claim 30; furthermore, Hamada discloses at least one of (a) said display data holding circuit [Fig. 4; TFT1 and C1] includes a thin film transistor [Fig. 4; TFT1] having a gate connected to the corresponding scanning electrode [Fig. 4; Y₁] and one of a drain and a source connected to the corresponding signal electrode [Fig. 4; X₁], and at least one (i) of a capacitor [Fig. 4; C1] at least partially formed by a portion of one of the drain and the source of said thin film transistor and

(ii) a static memory circuit connected to the other of the drain and the source of said thin film transistor, the static memory circuit including a plurality of thin film transistors, and (b) said display electrode is an opaque reflection electrode arranged in overlapping relation with at least one of said scanning electrode, said signal electrode, and a thin film transistor for enabling driving of the liquid crystal display apparatus in a reflection type display mode (see Column 7, Line 38 - Column 8, Line 45), wherein said display data holding circuit which includes a thin film transistor [Fig. 4; TFT1] having a gate connected to the corresponding scanning electrode [Fig. 4; Y₁] and one of a drain and a source connected to the corresponding signal electrode [Fig. 4; X₁] is provided, and a capacitor [Fig. 4; C1] is provided which is at least partially formed by a portion of one of the drain and the source of said thin film transistor (see Column 7, Line 38 -Column 8, Line 45).

Regarding claim 41, this claim is rejected by the reasoning applied in rejecting claims 30 and 40.

Regarding claim 42, this claim is rejected by the reasoning applied in rejecting claims 30 and 40.

Regarding claim 43, this claim is rejected by the reasoning applied in rejecting claims 30, 31, and 40.

Regarding claim 44, this claim is rejected by the reasoning applied in rejecting claims 30 and 40; furthermore, Hamada discloses one electrode of the capacitor is formed of a same material as a material of one of the drain and the source of said thin film transistor (see Fig. 4; Column 7, Line 38 - Column 8, Line 45).

Regarding claim 45, this claim is rejected by the reasoning applied in rejecting claim 31.

Response to Arguments

9. Applicants' arguments filed 15 October 2007 have been fully considered but they are not persuasive.

The Applicants contend, "[the instant] claims define one or more of the following features: 1) The drain of the thin film transistor of the display data holding circuit is connected to a corresponding signal electrode; 2) The capacitor of the display data holding circuit is at least partially formed by a portion of the drain of the thin film resistor; and 3) One electrode of the capacitor is formed of a same material as a material of the drain of the thin film transistor" (see Page 15 of the 'Amendment Under 37 CFR 1.114' filed on 15 October 2007). However, the examiner respectfully disagrees.

Hamada discloses a liquid crystal display apparatus (see the abstract), having a pair of substrates of which at least one substrate is transparent (see Column 6, Line 15) and a liquid crystal layer sandwiched between the substrates (see Column 1, Lines 20-21), comprising: a plurality of scanning electrodes [Fig. 4; Y] formed on one of the substrates (see Column 5, Line 55); and a plurality of signal electrodes [Fig. 4; X] intersecting in a matrix form with said

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plurality of scanning electrodes (see Figure 2 and Column 5, Line 54); wherein the display apparatus further comprises, within each of the regions surrounded by said plurality of scanning electrodes and said plurality of signal electrodes: (a) a display data holding circuit [Fig. 4; TFT1 and C1] connected to a corresponding scanning electrode [Fig. 4; Y₁] and signal electrode [Fig. 4; X₁], for fetching and storing display data from a signal electrode in response to a scanning signal (see Column 6, Lines 54-55) for holding a display image [in C1] without updating the display data [in C2] while a power supply [Fig. 4; Vc] to the display apparatus is maintained (see Column 6, Lines 59-65); (b) a switching device [Fig. 4; TFT2] connected to said display data holding circuit and having a switching operation thereof controlled by the display data holding circuit (see Column 6, Lines 59-65); and (c) a display electrode [Fig. 4; C2] connected to said switching device (see Column 5, Lines 66-68); wherein said display data holding circuit includes a thin film transistor [Fig. 4; TFT1] having a gate connected to the corresponding scanning electrode and one of a drain and a source connected to the corresponding signal electrode, and a capacitor [Fig. 4; C1] at least partially formed by a portion of one of the drain and the source of said thin film transistor (see Column 5, Lines 53-65 and Column 7, Line 38 - Column 8, Line 45), wherein

Hamada discloses the drain of the thin film transistor [Fig. 4; TFT1] of the display data holding circuit [Fig. 4; TFT1 and C1] is connected to the corresponding signal electrode [Fig. 4; X₁]; the capacitor [Fig. 4; C1] is at least partially formed by a portion of the drain of said thin film transistor [Fig. 4; TFT1]; and one electrode of the capacitor [Fig. 4; C1] is formed of a same material as a material of the drain of said thin film transistor (see Fig. 4; Column 7, Line 38 - Column 8, Line 45).

An "electrode" is merely a synonym for a "conductor." As is clearly evidenced by Hamada's Figure 4, a capacitor [Fig. 4; C1] is at least partially formed by a portion of one of the drain and the source of a thin film transistor [Fig. 4; TFT1] (see Column 7, Line 38 - Column 8, Line 45). The thin film transistor [Fig. 4; TFT1] is directly connected to the capacitor [Fig. 4; C1], and as such, they share a conductor (aka an "electrode" of the same material) therebetween.

Hamada does not expressly disclose the display data holding circuit having one of a coplanar and an inverse stagger structure.

However, Matsuda discloses thin film transistor circuits of a coplanar as well as an inverse stagger structure (see Column 1, Lines 49-54).

Hamada and Matsuda are analogous art because they are from the shared inventive field of using thin film transistor circuits for controlling liquid crystal elements.

Therefore, it would have been obvious to one skilled in the art at the time of invention to use Matsuda's coplanar or inverse stagger structure with Hamada's display data holding circuit, so as to manufacture the liquid crystal display apparatus with conventional, well known TFT design techniques (see Matsuda: Column 1, Lines 49-54).

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Piziali

20 December 2007